A Sol-Gel Derived (CoLi)Si_xO_y Thin Film for the Storage Layer of the Nonvolatile Flash Memory Device

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ABSTRACT

In this paper, a (CoLi)Si_xO_y thin film flash memory device was fabricated and demonstrated its electrical properties. The (CoLi)Si_xO_y thin film was formed using a simple sol-gel spin coating method, which has advantages such as low-cost, room temperature coating, and can be formed metal oxide film with multiple composite elements. The formed (CoLi)Si_xO_y thin film was verified by using tunneling electron microscope, and the electrical properties of the (CoLi)Si_xO_y flash memory devices regarding their transfer curves, operation speeds, reliabilities including retention and endurance, and stress disturbances, were discussed in this paper. The obtained results demonstrated that the (CoLi)Si_xO_y flash memory devices exhibited good performance, such as wide memory window, fast program/erase speeds, and low gate/drain disturbance characteristics.

I. INTRODUCTION

Nonvolatile memory devices have revolutionized the way we store and access data [1, 2]. Flash memory, which is one of the nonvolatile memory devices, has become a ubiquitous component of our everyday lives, powering everything from smartphones, embedded systems and artificial intelligence of things (AIOT) [3]. The importance of flash memory lies in their ability to retain data even when power is ceased, which makes them practical for applications where data storage is critical or ensure data is not lost in the event of power failure [4]. Flash memory devices also have advantages such as fast response time, low power consumption, and high reliability, making the flash memory attractive for many applications [5].

Conventional structure for the flash memory device uses a floating gate (FG) as the charge storage layer. The FG flash memory device possesses advantages like simple structure and fast program/erase speeds. Despite their many benefits, the FG flash memory devices encounter some limitations that have to be taken into consideration. One of the limitations of the FG flash memory is its shrinking capability to smaller feature sizes. Shrinkage of the feature sizes makes their reliability problems such as programming disturbance, read disturbance, and data retention loss [6, 7]. These shrinking induced issues become more pronounced at smaller feature sizes, thus retard widely applications of the FG flash memory devices because their performance and reliability. Moreover, as the density of flash memory increases, it becomes more difficult to achieve high performance and endurance while maintaining reasonable cost and power consumption [8].

Another structure for the flash memory device is silicon-oxide-nitride-oxide-silicon (SONOS), which uses Si_3N_4 as the charge storage layer [9]. The dielectric constant of Si_3N_4 is 7.5 eV and possesses 2.05 eV barrier height versus silicon. The SONOS flash memory device has better charge retention storage than FG structure because of its discrete trap centers diversely with the thin tunnel oxide [10]. However, the challenge for SONOS structure is its programming speed. In addition, small barrier height of Si_3N_4 film to silicon may also induces data retention issue because the trapped charges thermally de-trapped from this shallow well easily. For the reasons mentioned above, high-k materials such as ZrO_2 or HfO_2 are proposed to replace Si_3N_4 film in the SONOS flash memory [11, 12]. The high-k materials have to perform high P/E speed, long retention/endurance storage, and little disturbance characteristics for the flash memory.

In this paper, we present sol-gel spin coating technique to deposit composited metal oxide high-k materials as the charge trapping layer in the flash memory device. Compare to other deposition methods, the Sol-Gel spin coating method have many merits, including low cost, convenient, low temperature fabrication, and easy to synthesize composite materials [13]. In addition, the sol-gel method can easily be done in a normal environment, no need for high vacuum and expensive equipment [14].

A ternary metal oxide materials (CoLi)Si_xO_y thin film was fabricated in this study by using sol-gel spin coating method. The (CoLi)Si_xO_y thin film was applied in the flash memory devices, serving as the

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charge trapping layer in the SONOS structure. We examined the electrical properties of the (CoLi)Si_xO_y flash memory devices including current-voltage transfer curves, operation speeds, reliability and disturbance issues. The obtained results demonstrate that the (CoLi)Si_xO_y flash memory devices exhibit large memory window, fast program/erase speed, long data retention, high endurance cycles, and stable in disturbance characteristics. The results indicated (CoLi)Si_xO_y thin film is a good candidate for the charge trapping layer of flash memory devices.

II. MATERIALS AND EXPERIMENTS

1. Sol-gel (CoLi)Si_xO_y thin film coating

($CoCl_2 \cdot 6H_2O$) (99.5%), $LiClO_4$ (99.5%), and $SiCl_4$ (99.5%), which were used as the precursors of the sol-gel solution, were purchased from Aldrich. Firstly, $CoCl_2 \cdot 6H_2O$), $LiClO_4$, and $SiCl_4$ powders were solved in 2-propanol (IPA) solvent respectively with ice-bath to avoid aggregation. The precursors used in sol-gel process including metal or metalloid were surrounded by different kinds of reactive ligands. The precursor solution was stirred vigorously for 30 min to remain its homogeneous state. Those solutions were then mixed together with ($CoCl_2 \cdot 6H_2O$) : $LiClO_4$: $SiCl_4$: IPA = 1:1:1:1000 in molar ratio, and stirred for 30 min to prevent precipitation.

To form a sol-gel thin film, the precursor solution were spin-coated on the silicon substrates at rotation speed of 3000 rpm for 60 sec. by using Tokyo Electron Limited spin coater system (Clean Track model-MK8). After spin-coating, these samples were subjected to rapid thermal anneal at 1050 °C for 60 sec in an O_2 ambient. This process was to ensure the gel film transferred into a solid thin film of spinodal decomposition. The flow chart of sol-gel process to form the (CoLi)Si_xO_y thin film is depicted in Figure 1.

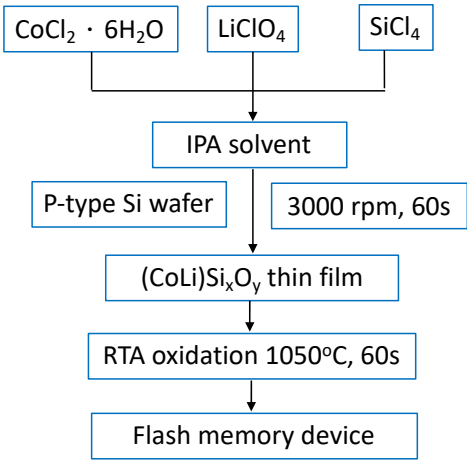

Figure 1. Flow chart of the (CoLi)Si_xO_y thin film fabrication by using sol-gel spin coating to form the flash memory device.

2. Flash memory device fabrication

The nonvolatile flash memory device was fabricated using standard MOSFET process. A 6 inch, p-type (100) silicon wafer was used as the substrate. Firstly, a stack film of SiO_2/Si_3N_4 was deposited, and then the 1st pattern was defined. A wet oxidation process was conducted to form SiO_2 isolation, while area where the Si_3N_4 exposed did not form oxide film because the Si_3N_4 was dense for oxygen to penetrate. As a result, a local oxidation of silicon (LOCOS) was done. After SiO_2/Si_3N_4 was removed, a high quality 5-nm SiO_2 film was formed to serve as gate oxide by using dry oxidation, the sol-gel precursor solution with the same concentration mention above was spin coated on the gate oxide, followed by a rapid thermal oxidation process at 1050 °C for 60 sec to form a stable (CoLi)Si_xO_y thin film, then a 30-nm blocking oxide was deposited. A 200-nm polycrystalline silicon film was continuously formed. The 2nd mask was performed to form the gate structure, then As^+ ion implantation was executed for lightly-doped drain. A TEOS oxide was deposited and etched back to from sidewall spacer, followed by 2nd As^+ ion implantation and rapid thermal anneal were conducted to form source/drain. A 500-nm-thick TEOS oxide was deposited and then 3rd mask was performed to define contact hole. After dry etch process to open the contact hole, a Ti/TiN/AlSiCu/TiN stack layer of metal pad was deposited. Finally, the 4th mask was performed, followed by metal dry etch process to define the metal electrodes of source, drain, and gate. The schematic presentation of the fabricated sol-gel flash memory devices is depicted in Figure 2.

The microstructure of the (CoLi)Si_xO_y thin film was examined using high resolution transmission electron microscopy (HRTEM). The electrical characteristics of the flash memory devices were measured using an Agilent 4156 semiconductor parameter analyzer. The feather sizes of the measured devices reported in this paper had a channel width and length of 10 and 0.35 μm, respectively.

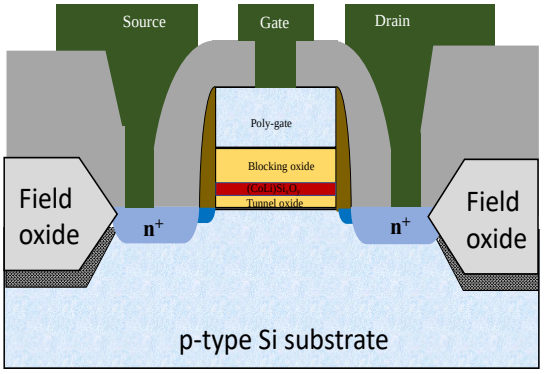

Figure 2. Schematic diagram of the flash memory structure by using sol-gel derived (CoLi)Si_xO_y thin film as the storage layer.

III. RESULTS AND DISCUSSION

Figures 3 depicts the cross sectional HRTEM image of the (CoLi)Si_xO_y thin film formed on SiO_2 and after 1050 ^oC 60 sec RTO anneal. The average thickness of the sol-gel derived (CoLi)Si_xO_y thin film is around approximately 3 nm. The fabricated thin film shows a very smooth interface, indicates that high quality of the (CoLi)Si_xO_y thin film by using sol-gel method, and is suitable for flash memory applications.

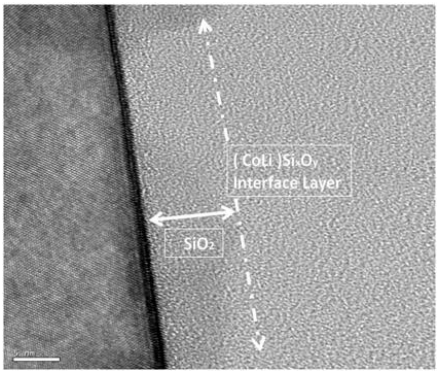

Figure 3. HRTEM image of the (CoLi)Si_xO_y thin film on SiO_2 after 1050^o C anneal for 60 sec.

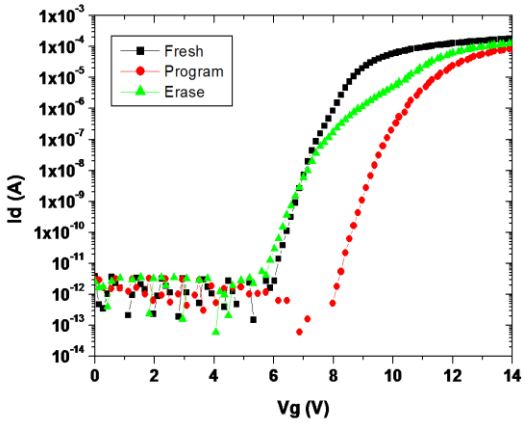

Figure 4. I_d-V_g curves of the sol-gel derived (CoLi)Si_xO_y flash memory devices at fresh, program, and erase states.

Figure 4 shows the drain current versus gate voltage (I_d-V_g) characteristics of the MOSFET device using (CoLi)Si_xO_y thin film as the charge storage layer of the flash memory. The black, red and green curves shown in the figure represented the flash memory device operated under fresh, program and erase states, respectively. The I_d-V_g curves of the memory device is very similar to that of MOSFET device, and the on/off current ratio can be up to 8 orders of magnitude. For programming operation, the channel hot electron injection (CHEI), and V_g = 10 V and drain voltage (V_d) = 9 V with 100 ms stress was applied to the memory device [15]. For erasing operation, band-to-band hot hole injection (BBHHI), and V_g = −6 V and V_d = 10 V with 10 ms stress was used [16]. For the device at fresh state, the threshold voltage (V_{th}) was estimated to be 6.8 V. After programming operation, the transfer curve shifted to right, and the V_{th} was increased to 10.1 V. As the device was applied erasing operation, the curve shift back to the original position. The memory window of the (CoLi)Si_xO_y flash memory device was 3.3 V, which was larger than other memory devices reported previously [17].

Figure 5 shows the program speeds of the (CoLi)Si_xO_y flash memory device under various operating conditions. Here the CHEI method was also used for programming operations, and the applied voltages were: (1) V_g = 8 V, V_d = 8 V, (2) V_g = 9 V, V_d = 9 V, and (3) V_g = 10 V, V_d = 9 V. The obtained results indicate that the V_{th} shift increases when the programming time is increasing. The same results can also be observed as the the applied V_g is increased. All the results could be explained by the phenomenon of hot electrons injection. That is, when increasing programming time or gate voltage, more energy applied to the to the flash memoey devices, then more hot electrons was injected through gate oxide and into the (CoLi)Si_xO_y trapping layer [21]. The largest V_{th} shift could reach up to ~5 V for V_d = 10 V, V_g = 9 V and 1-s programming operation.

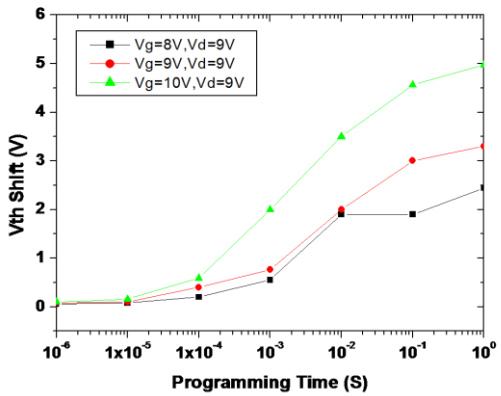

Figure 5. Program speed characteristics of the (CoLi)Si_xO_y flash memory device under different operation conditions.

Figure 6 shows the erase speed properties of the (CoLi)Si_xO_y flash memory device under various operating conditions. The erase speed properties were measured by using BBHHI method, ans the operating conditions were: (1) V_g = −9 V, V_d = 9 V, (2) V_g = −10 V, V_d = 9 V, and (3) V_g = −6 V, V_d = 10 V. At the erase operation, the memory device was from SET back to RESET, thus the I_d-V_g shifts leftward, the value of V_{th} shift was negative. Same as program spped, the V_{th} shift increases when the erasing time is increasing. Moreover, the results show that both the V_g and V_d influence the erase speed, especially the voltage of V_d. This rrsult might caused by the effective electric field of V_d to eliminate electrons from the charge trapping layer in the BBHHI operation. The largest V_{th} shift

could reach up to −4 V for V_g = −6 V, V_d = 10 V and 1-s erasing operation.

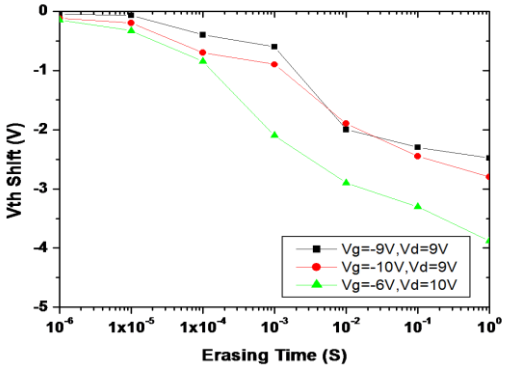

Figure 6. Erase speed characteristics of the (CoLi)Si_xO_y flash memory device under different operation conditions.

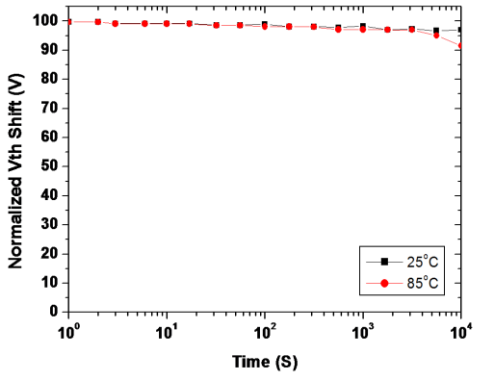

Figure 7. Data retention of the (CoLi)Si_xO_y flash memory device at 25 and 85 ℃ operations.

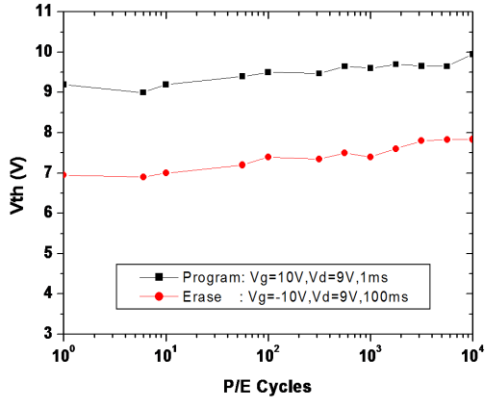

Figure 8. Endurance of the (CoLi)Si_xO_y flash memory device under different operation conditions.

The reliability characteristics of the (CoLi)Si_xO_y flash memory device were also demonstrated in this paper. Figures 7 and 8 present retention and endurance characteristics of the proposed memory device, respectively. The retention measurements of the memories were carried out from 1-10000 s under 25 and 85 °C conditions. For the device under 25 °C measurement, only 5% charge loss was observed at 10^4 s retention time, and approximately 10% charge loss of the flash memory device under 85 °C measurement. The (CoLi)Si_xO_y flash memory device exhibits excellent retention properties even at 85 °C and long duration time, indicates the sol-gel derived (CoLi)Si_xO_y thin film is very suitable to serve as the charge trapping layer. The endurance characteristic of the (CoLi)Si_xO_y flash memory device for 10^4 program/erase (P/E) switching times was shown in Figure 8. In this measurement, pulse voltages of V_g = 10 V and V_g = 9 V for 1-ms were used for programming, and pulse voltages of V_g = −10 V and V_d = 9 V for 100-ms were for erasing operation. As shown in the figure, both the V_{th} of program and erase increase as the (P/E) switching times is increasing. The V_{th} of the program state is from 7 V to 7.7 V, whereas the V_{th} of the erase state is from 9.2 V to 10.0 V, after 10^4 cycle times. The V_{th} shift is higher in the erase state than in the program state, implies that the applied voltage might be excess during erasing operation [18].

Disturbance properties of the (CoLi)Si_xO_y flash memory device, including the gate and drain disturbances, were also conducted in this paper. The disturbance properties, which are associated with the device reliability, are more and more important because of the integration concern of the memory array [19]. The density of the memory devices is getting increase, as a result, operation on a device may influence the properties of surrounding memory devices [20]. Figure 9 presents the gate disturbance characteristic of the (CoLi)Si_xO_y thin film flash memory device. The gate disturbance was measured for the memory device was in the erase state, and the gate voltage stresses were applied at V_g = 8 V and 9 V. As shown in the figure, the V_{th} almost unchanged when the device was under voltage stress at V_g = 8 V for 10^3 s, whereas for the V_g = 9 V operation, V_{th} shifted by only 0.26 V for 10^3 s.

The drain disturbance characteristics of the (CoLi)Si_xO_y thin film flash memory device is shown in Figure 10. The drain disturbance measurement was also conducted in the erase state, and the stress in the drain was applied at V_d = 9 V and 10 V. Similar results were obtained for V_d = 9 and 10 V stress at 10^3 s, that the V_{th} shifts were around only 0.03 V. The disturbance characteristics of the (CoLi)Si_xO_y flash memory devices exhibit excellent performance, indicates the (CoLi)Si_xO_y thin film is stable to serve as the charge trapping layer for the flash memory devices.

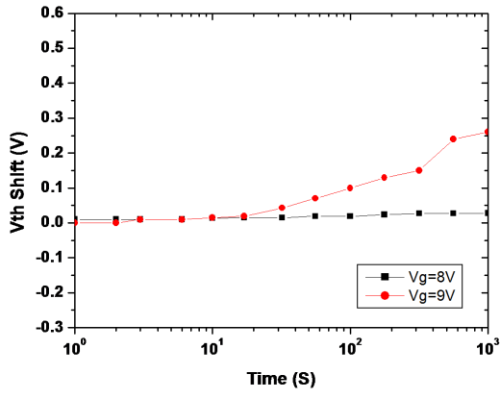

Figure 9. Gate disturbances of the (CoLi)Si_xO_y flash memory device under different operation conditions.

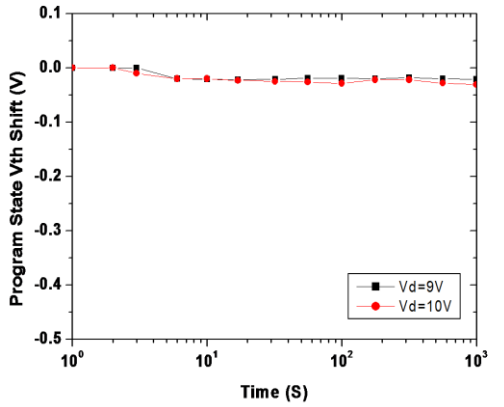

Figure 10. Drain disturbances of the (CoLi)Si_xO_y flash memory device under different operation conditions.

IV. CONCLUSIONS

In this paper, a facile (CoLi)Si_xO_y thin film was formed by using simple sol-gel spin coating method. The (CoLi)Si_xO_y thin film was applied to serve as the charge trapping layer of a flash memory device. The cross sectional electron microscopy image demonstrated the smooth and uniform thin film formed on SiO_2 layer. The electrical properties of the (CoLi)Si_xO_y flash memory devices regarding the I_d-V_g curves, program and erase speeds, retention, endurance, and disturbances were measured. The program/erase memory window of the (CoLi)Si_xO_y flash memory device could be up to 3.3 V. For the P/E speed, the V_{th} shift could reach to 2 V at 10^{-3}-s programming for V_d = 10 V and V_g = 9 V, and -2 V at 10^{-3}-s erasing for V_g = −6 V and V_d = 10 V operation. The reliability and disturbance characteristics also exhibited excellent performace, indicated that the (CoLi)Si_xO_y flash memory devices is suitable for a good and stable metal oxide composite flash memory.

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REFERENCES

[1] R. Kawashima, H. Nohira, R. Ishikawa *et al.*, "Fabrication of metal/oxide/fluorographene/oxide/silicon capacitors and their charge trapping properties," Japanese Journal of Applied Physics, Vol. 62, No. Sg, 2023.

[2] D. Kwon, J. H. Jung, C. J. Kang *et al.*, "Neurotransmitter ligand effect of dopamine and cortisol conjuation on ZnO nanoparticles embedded polyvinylphenol resistive switching device," Materials Science in Semiconductor Processing, Vol. 160, 2023.

[3] C.-C. Wu, Y.-J. Tsai, P.-L. Liu *et al.*, "Facile sol–gel preparation of nanocrystal embedded thin film material for memory device," Journal of Materials Science: Materials in Electronics, Vol. 24, No. 1, pp. 423-430, 2012.

[4] S. H. Liu, W. L. Yang, C. C. Wu *et al.*, "A Novel Ion-Bombarded and Plasma-Passivated Charge Storage Layer for SONOS-Type Nonvolatile Memory," IEEE Electron Device Letters, Vol. 33, No. 10, pp. 1393-1395, 2012.

[5] D. W. Kang, H. Park, D. H. Kim *et al.*, "Device characteristics of the select transistor in a vertical-NAND flash memory," Japanese Journal of Applied Physics, Vol. 62, No. 2, 2023.

[6] D. Spassov, A. Paskaleva, E. Guziewicz *et al.*, "Charge Storage and Reliability Characteristics of Nonvolatile Memory Capacitors with HfO2/Al2O3-Based Charge Trapping Layers," Materials, Vol. 15, No. 18, 2022.

[7] S. J. Wang, G. Y. Geng, Y. Sun *et al.*, "Flash memory based on MoTe2/boron nitride/graphene semi-floating gate heterostructure with non-volatile and dynamically tunable polarity," Nano Research, Vol. 15, No. 7, pp. 6507-6514, 2022.

[8] X. Y. Yu, Z. Y. Ma, Z. X. Shen *et al.*, "3D NAND Flash Memory Based on Double-Layer NC-Si Floating Gate with High Density of Multilevel Storage," Nanomaterials, Vol. 12, No. 14, 2022.

[9] Y. M. Chang, W. L. Yang, S. H. Liu *et al.*, "A hot hole-programmed and low-temperature-formed SONOS flash memory," Nanoscale Research Letters, Vol. 8, 2013.

[10] C. Y. Wu, H. Y. Huang, and C. C. Wu, "Low-Temperature Formed Quaternary NiZrSiGe Nanocrystal Memory," International Journal of Electrochemical Science, Vol. 10, No. 8, pp. 6500-6508, 2015.

[11] J. Choi, J. Bae, J. Ahn *et al.*, "Electrical

characteristics of SiO2/ZrO2 hybrid tunnel barrier for charge trap flash memory," Japanese Journal of Applied Physics, Vol. 56, No. 8, 2017.
[12] W. Banerjee, A. Kashir, and S. Kamba, "Hafnium Oxide (HfO2) - A Multifunctional Oxide: A Review on the Prospect and Challenges of Hafnium Oxide in Resistive Switching and Ferroelectric Memories," Small, Vol. 18, No. 23, 2022.
[13] C. C. Wu, Y. J. Tsai, P. L. Liu *et al.*, "Facile sol-gel preparation of nanocrystal embedded thin film material for memory device," Journal of Materials Science-Materials in Electronics, Vol. 24, No. 1, pp. 423-430, 2013.
[14] M. S. Huang, V. Suresh, M. Y. Chan *et al.*, "Multi-layered metal nanocrystals in a sol-gel spin-on-glass matrix for flash memory applications," Materials Chemistry and Physics, Vol. 186, pp. 36-43, 2017.
[15] A. Goda, "3-D NAND Technology Achievements and Future Scaling Perspectives," Ieee Transactions on Electron Devices, Vol. 67, No. 4, pp. 1373-1381, 2020.
[16] [. H. Lin, M. S. Yeh, Y. R. Jhan *et al.*, "Band-to-Band Hot Hole Erase Mechanism of p-Channel Junctionless Silicon Nanowire Nonvolatile Memory," IEEE Transactions on Nanotechnology, Vol. 15, No. 1, pp. 80-84, 2016.
[17] S. D. Yang, J. K. Jung, J. G. Lim *et al.*, "Investigation of Intra-Nitride Charge Migration Suppression in SONOS Flash Memory," Micromachines, Vol. 10, No. 6, 2019.
[18] T. P. Xiao, B. Feinberg, C. H. Bennett *et al.*, "An Accurate, Error-Tolerant, and Energy-Efficient Neural Network Inference Engine Based on SONOS Analog Memory," Ieee Transactions on Circuits and Systems I-Regular Papers, Vol. 69, No. 4, pp. 1480-1493, 2022.
[19] X. L. Jia, L. Jin, J. Q. Jia *et al.*, "A Novel Program Scheme to Optimize Program Disturbance in Dual-Deck 3D NAND Flash Memory," IEEE Electron Device Letters, Vol. 43, No. 7, pp. 1033-1036, 2022.
[20] Y. Cai, Y. X. Luo, S. Ghose *et al.*, "Read Disturb Errors in MLC NAND Flash Memory," Ipsi Bgd Transactions on Internet Research, Vol. 14, No. 2, 2018.

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