Five-Transistor SRAM Cell with Improved Write Capability

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Abstract

In this paper, we propose a five-transistor (5T) static random access memory (SRAM) that can be read and written reliably with the assistance of read/write circuits. The read/write circuits include a voltage control circuit, a pre-charging circuit and a standby start-up circuit. The voltage control circuit is connected to the sources corresponding to driver transistors of each row memory cells. This configuration is aimed to control the source voltages of driver transistors under different operating modes. Specifically, in a write mode, the issue concerning the difficulty of writing a logic '1' can be avoided. In a read mode, the reading speed can be increased without incurring unnecessary power consumption. In a standby mode, leakage current can be reduced effectively. In addition, each column memory cells set up a pre-charging circuit, and each pre-charging circuit is connected to the bit line BL of the corresponding column memory cells. Moreover, the standby start-up circuit design enables the single-port SRAM to quickly switch to the standby mode, which effectively enhances the standby performance of the single-port SRAM.

Keywords: static random access memory, read/write assist circuit, voltage control circuit, standby start-up circuit.

1. Introduction

Memory plays an essential role in computer industries. Usually, static random access memories (SRAMs) are used in applications requiring high speed, such as memory in a data processing system.

SRAM cells use a write operation to store data in the cell and a read operation to sense the data stored in the cell. As such, the SRAM cell should provide good stability during read operations without harming speed or the ability to write to the cell.

Figure 1 is a circuit diagram of a conventional six-transistor (6T) SRAM cell. The memory cell includes a pair of cross-coupled inverters and a pair of access Transistors, MA1 and MA2. The pair of cross-coupled inverters are formed by a pair of load transistors, MP1 and MP2, and a pair of driver transistors, MN1 and MN2, that are stronger than the access transistors. In particular, one inverter is coupled to bit line BL through access transistor MA1, and the other inverter is coupled to complementary bit line BLB through access transistor MA2. More specifically, the cross-coupled inverters of the memory cell have two storage nodes, A and B, functioning to store either a logic '1' or a logic '0'. In general, a 6T SRAM cell is accessed through both of access transistors during reading and writing operations. During the reading and writing operations, different voltages must be applied to the bit lines. The gates of access transistors are connected to a word line WL.
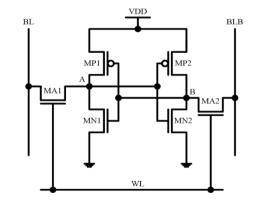

Figure 1: Circuit diagram of conventional 6T SRAM cell.

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During the accessing operations, the word line WL is asserted to make transitions from a logic low to a logic high. At the end of operations, the word line voltage is reduced to ground allowing the cross-coupled inverters to function normally and hold the logic state of the storage nodes. Accessing a SRAM cell in this manner leads to a relatively stable SRAM cell during both reading and writing operations. The reading and writing operations of a SRAM cell are well documented in numerous resources [1], and will not be described further.

It is well known that the cell ratio has an effect on access speed and on cell stability. For stabilization of a reading operation, the cell ratio between the driver and access transistors was conventionally set at 2 to 3 or more [2], and the driver transistors should be designed to have a larger gate width, which also causes an increase in size of the memory cell of the SRAM [3]. Therefore, higher integration and lower cost cannot be expected with a conventional 6T SRAM.

Further, although the SRAM does not require the refresh operation, a relatively large layout area is required for the six transistors of SRAM cell. Therefore, it would be desirable to have an SRAM cell that requires fewer than six transistors, but it has the same stability as a 6T SRAM cell.

In this paper, the proposed 5T SRAM has the following advantages compared to the existing 6T SRAMs:

1) Avoiding the difficulty in writing a logic '1' operation without impeding the reading operation;
2) Faster reading speed;
3) Quickly switching to the standby mode;
4) Lower standby current;
5) Fewer total transistor count.

The remainder of this paper is organized as follows. Section 2 presents a brief description of a conventional 5T SRAM cell. The proposed 5T SRAM cell is described in Section 3. A detailed description of the writing operation and the simulation results of the proposed 5T SRAM cell are discussed in Section 4. Last section is a conclusion and summary for the paper.

2. Existing 5T SRAM Cell

Figure 2 is a circuit diagram of a conventional five-transistor (5T) SRAM cell [4-5]. As shown in Figure 2, access transistor MA2 and bit line BLB in Figure 1 have been removed to provide a five-transistor configuration. The removal of such access transistor allows for an area savings up to 20-30% compared to the 6T SRAM cell, while its power consumption is substantially reduced by one half [6]. The drain of access transistor MA1 is coupled to the drains of transistor MP1 and transistor MN1, which is identified as storage node A. The voltage at node A determines the bit stored in memory cell; that means that a voltage of approximately VDD is read as a logic '1', and a voltage of approximately ground voltage is read as a logic '0'. Data to and from the 5T memory cell is controlled by activating the word line WL of the single access transistor MA1 to the single bit line BL and storage node A. Consequently, only one side of the SRAM cell is accessed for reading and writing data to the cell. In order to achieve a reliable writing, it may be necessary that the access transistor should be very conductive to force the cross-coupled inverters to change its equilibrium condition [7]. However, the access transistor should have a reduced conductivity for good stability in reading and standby operations.
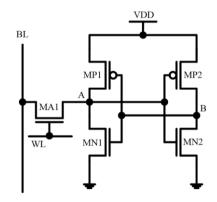

Figure 2: Circuit diagram of conventional 5T SRAM cell.

As mentioned above, although conventional single-port 5T SRAM cells offer such significant reductions in power consumption, a serious drawback is aroused in that it is difficult to write a logic '1' to a memory cell that is storing a logic '0' [6], [8-10]. In more detail, access transistor MA1 is less conductive than driver transistor MN1, thereby making it more difficult to write a logic '1' to memory over a logic '0' stored. The simulated waveform of the writing operation cycle is shown in Fig. 3.
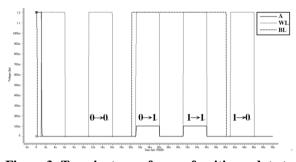

Figure 3: Transient waveforms of writing a data to the conventional 5T SRAM cell.

In order to obtain a reliable writing, several techniques have been developed to solve the write '1' issue in 5T SRAM cells; these techniques, for example, include the source supply voltage of the memory cells by a specific voltage below the power supply voltage VDD [11-13], asymmetrical SRAM cells with asymmetrical cell transistor sizing [14-15], the word line WL voltage boosted ter than the power supply voltage VDD [16-17], raising the source voltage of driver transistor MN1 higher than the ground voltage [7], and so on. However, each of these techniques may cause a reduction in the drive current of the transistors and in the operating speed of the circuit, or has increased memory cell area and a degradation in the manufacturing accuracy, or requires generation of a voltage above the operating voltage, or requires a more complicated circuit design and more complicated device process.

SRAM memory cells may also be unstable. That is, the data in the cells may be corrupted when the cells are read [18]. Actually, a higher voltage on the bit line is coupled to a lower voltage in the cell, causing the bit line voltage to drop and the cell voltage to rise. However, since a logic '0' stored initially, the voltage rise in the cell may corrupt the data stored. It would clearly be desirable to provide a

design for an SRAM cell that is more stable than conventional designs and is, therefore, less likely to be corrupted when the cell is read.

In view of these drawbacks, it is the object of the paper to remove the above-mentioned drawbacks and to provide a SRAM cell with reliable writing and stable reading. It is a further object of the paper to provide a SRAM cell with fast read, fast write and low power dissipation.

3. Proposed 5T SRAM Cell

3.1 Proposed 5T SRAM Cell Configuration

The configuration of the proposed 5T SRAM is stated as follows. Memory cells, shown in Figure 4, are arranged in arrays. Beyond arrays, there are read/write assist circuits, for example, voltage control circuits, pre-charging circuits, and standby start-up circuits, which process data read/write operations. The standby start-up circuit design is to enable the single-port SRAM to quickly switch to the standby mode, and thus effectively to enhance the standby performance of the single-port SRAM. In addition, each row memory cells set up a voltage control circuit, and each voltage control circuit is connected to the source terminals of the pair of driver transistors. In this design, memory cells in the same row are asserted by the same word line WL, and memory cells in the same column use the same bit line BL to perform data read/write operations. For the simplicity of the description, in the following description, the reference is 1-bit memory cell, as illustrated in Figure 4.
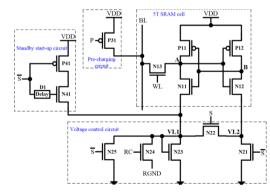

Figure 4: Circuit diagram of the proposed 5T SRAM cell.

In this design, during a write operation, the write line WL is asserted, and transitions are switched from a logic '0' to a logic '1'. A voltage at the source of the driver transistors is pull-down to ground, thus making it easier for the stored data at the storage node A to change. At the end of the write operation, the word line voltage is reduced to ground allowing the cross-coupled inverters to function normally and hold the logic state of the storage node.

To write a logic '0' to SRAM cell, the supply voltage VDD is applied to word line WL, and the ground voltage is applied to bit line BL. Under these conditions, access transistor MA1 is turned on, and a voltage equal to the ground voltage is applied to node A. Alternatively, to write a logic '1' to a SRAM cell, the supply voltage VDD is applied to both bit line BL and word line WL. Consequently, access transistor MA1 is turned on, and a voltage equal to VDD-Vtn is applied to node A, where Vtn is the threshold voltage of access transistor MA1. It is worth noting that the channel W/L ratio of transistor N11 is designed smaller than that of transistor MN1 as shown in Figure 1. Therefore, the difficulty of overwriting a logic '1' to a logic '0' problem associated with the conventional 5T SRAM cell can be solved.

Next, during a read operation, due to the source voltage of driver transistor N11 is pulled down to lower than the ground voltage, and the channel W/L ratio of transistor N11 is designed smaller; thus, these conditions can speed up the reading speed without impeding the reading operation.

3.2 Proposed Read/Write Assist Techniques

As can be seen in Fig. 4, the standby start-up circuit is connected to the source of transistor N11 in a selected row memory cells. The standby start-up circuit design enables the single-port SRAM to quickly enter standby mode, which effectively enhances the standby performance of the single-port SRAM. Furthermore, the voltage control circuit is connected to the source terminals corresponding to driver transistors of each memory cell in selected row memory cells. This configuration is aimed to control the source voltages of driver transistors under different operating modes. Specifically, during a

write operation, the voltages of nodes VL1 and VL2 are set to the ground voltage, so the issue concerning the difficulty of writing a logic '1' can be prevented. During a read mode, the voltage of node VL1 is set to a speed-up reading voltage RGND that is lower than the ground voltage. Under this circumstance, the speed-up reading voltage RGND can effectively improve the reading speed without incurring unnecessary power consumption. Also, this technique in which speed-up reading voltage RGND is lower than ground voltage is more efficient in reducing leakage current than the one in which ground voltage is increased. Table 1 summaries the voltage level under different operating modes.

Table 1: The voltage level under different modes

mode	RC	S	VL1	VL2
write	RGND	0	0	0
read	VDD	0	RGND	0
standby	RGND	VDD	$V_{GS(N23)}$	$V_{GS(N23)}$
hold	RGND	0	0	0

In Table 1, the read control signal RC can be achieved by performing the AND operation on the read enable signal RE (not shown) and its corresponding word line signal WL. It is worth noting that the non-selected word line and non-selected bit line are set to the floating state. However, in the non-reading mode, the voltage of read control signal RC is set to the speed-up reading voltage RGND that is lower than the ground voltage. This technique yields the maximum reduction in leakage current caused by transistor N24.

3.3 Write Operation

Figure 5 shows the simplified circuit diagram during the write operation. By this configuration, before and during the write operation is executed, the standby start-up control signal S is at a logic '0'; therefore, transistor N25 is turned on, so the voltage of the node VL1 is pulled down to ground voltage. During the write '0' operation, the voltage of bit line BL is pulled down to a logic '0', and the asserted word line WL turns on transistor N13. Thus, node A is at a logic '0' , and node B is at a logic '1'. Conversely, during the write '1' operation, the voltage of bit line BL is pulled up to a logic '1' , and the asserted word line WL turns on transistor N13.

Thus, node A is at a logic '1' , and node B is at a logic '0'. It is worth noting that the channel W/L ratio of transistor N11 in Figure 4 is designed smaller than that of transistor MN1 as shown in Figure 1. Consequently, the problem associated with the conventional 5T SRAM cell for write '1' operation can be avoided.
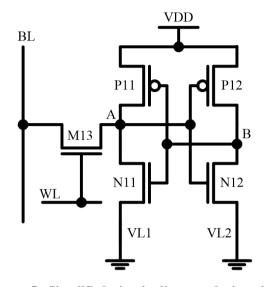

Figure 5: Simplified circuit diagram during the write operation.

3.4 Read Operation

Figure 6 shows the simplified circuit diagram during the read operation. Before the read operation is executed, both the standby start-up control signal S and the read control signal RC are at logic '0', so transistor N25 is turned on and transistor N25 is turned off; therefore, the voltage of node VL1 is pulled down to the ground voltage.
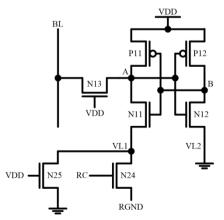

Figure 6: Simplified circuit diagram during the read operation.
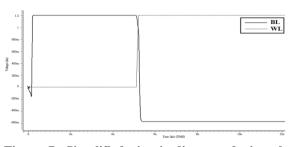

Figure 7: Simplified circuit diagram during the read operation.

During the read operation, the read control signal RC is at logic '1', so transistor N24 is turned on; therefore, the voltage of node VL1 is pulled down to a speed-up reading voltage RGND that is lower than the ground voltage, as shown in Figure 7. Under this circumstance, the speed-up reading voltage RGND can effectively improve the reading speed.

3.5 Standby Operation

Figure 8 shows the simplified circuit diagram during the standby operation. Prior to the standby operation is executed, the inverse standby control signal /S is at logic high that will cause transistor P41 to turn off and transistor N41 to turn on. And then, during the standby operation, the inverse standby control signal /S is at logic low to turn on transistor P41 and to turn off transistor N41. However, at the beginning of the standby operation, transistor N41 still turned on, so this leads to the voltage of node VL1 can be rapidly charged to the threshold voltage of transistor N23. That is, the SRAM cell can switch rapidly to the standby mode and, thereby, improve the standby efficiency. It is worth noting that transistor N41 is turned off, and no current is supplied, after the initial period of the standby operation.

During a standby operation, the standby control signal S is at logic high to turn on transistor N22 and to turn off transistor N21, so the voltage of node VL1 is equal to that of node VL2. Consequently, the voltage of these two nodes is the same as the threshold voltage of transistor N23.
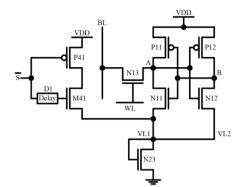
Figure 8: Simplified circuit diagram during the standby operation.

4. Simulation Results and Discussion

4.1 Simulation Results

To evaluate performance, different SRAM cell structures discussed in this paper were designed using a 90 nm CMOS technology. Figure 9 illustrates a timing diagram to perform a write operation from the five-transistor SRAM cell. With reference to Figure 9, the WL and the BL voltage levels are shown.

All simulations are carried out at nominal conditions: VDD=1.2V and at room temperature. The simulated waveform of writing a data value to the proposed 5T SRAM cell is shown in Figure 10. It is evident that the proposed SRAM cell provides an efficient solution to the write '1' issue, that is, the proposed 5T SRAM cell enabling a logic '1' to be easily written to the SRAM cell, as compared to conventional 5T SRAM cells.
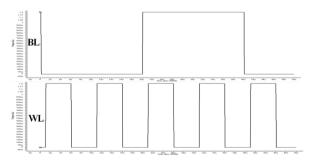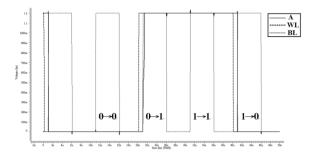

Figure 9: Timing diagram to perform a write operation.

Figure 10: Transient analysis waveforms of writing a data value to the proposed 5T SRAM cell

4.2 Discussion

As shown in Figs. 5 and 10, there are four cases for the write operation. The transients associated with these four cases are described in detail below.

4.2.1 Write a Logic '0' to a Logic '0' Stored

In this case, before the writing operation begins, transistors P11 and N12 are turned off, and transistors P12 and N11 are turned on. When the write '0' operation is executed, the word line WL is asserted, and transitions are switched from a logic low to a logic high. As the word line WL with a voltage exceeding the threshold voltage of transistor N13, transistor N13 will be turned on. At this time, since the bit line BL is at logic '0', node A is discharged and forced to the ground voltage. As a result, node A maintains its logic '0' voltage level throughout the write '0' cycle.

4.2.2 Write a Logic '1' to a Logic '0' Stored

In this case, before the write operation begins, transistors P11 and N12 are turned off, and transistors P12 and N11 are turned on. When the write '0' operation is executed, the word line WL is asserted, and transitions are switched from a logic low to a logic high. As the word line WL with a voltage exceeding the threshold voltage of transistor N13, transistor N13 will be turned on. At this time, since the bit line BL is at logic '1', transistor N11 is still turned on, and transistor P11 is still turned off. Meanwhile, node A can be charged toward $VDD \times (R_{N11}/(R_{N11}+R_{N13}))$ by the voltage dividing effect between N11 and N13, wherein R_{N11} is the on-resistance of transistor N11, and R_{N13} is the

on-resistance of transistor N13, respectively. Since the channel W/L ratio of transistor N11 in Figure 4 is designed smaller than that of transistor MN1 as shown in Figure 1, so that the read operation does not impede. In addition, by this design, it enables the divide voltage higher than the threshold voltage of transistor N12. Consequently, N12 is turned on, and node B is discharged to a lower voltage level. Meanwhile, node A rises since transistor N11 now possess higher resistance value. This higher resistance value helps pull up node A toward higher voltage level. And then, by using inverter (P12, N12), this higher voltage level on node A will pull node B down to much lower voltage level. Furthermore, by using inverter (P11, N11), this much lower voltage level on node B will pull node A up to much higher voltage. Then, repeating these two operations alternately, node B falls to ground voltage, and node A is pulled up to VDD to accomplish the write '1' operation.

4.2.3 Write a Logic '1' to a Logic '1' Stored

In this case, before the write operation, transistors P11 and N12 are turned on, and transistors P12 and N11 are turned off. When the write '1' operation is executed, the word line WL is asserted, and transitions are switched from a logic low to a logic high. As the word line WL with a voltage exceeding the threshold voltage of transistor N13, transistor N13 will be turned on. At this time, since the bit line BL is at logic '1' , and transistor N11 is still turned on, node A maintains its logic '1' potential stably throughout the whole write '1' cycle.

4.2.4 Write a Logic '0' to a Logic '1' Stored

In this case, before the write operation, transistors P11 and N12 are turned on and transistors P12 and N11 are turned off. When the write '0' operation is executed, the word line WL is asserted and transitions from a logic low to a logic high. As the word line WL with a voltage exceeding the threshold voltage of transistor N13, transistor N13 will be turned on. At this time, since the bit line BL is at logic '0', node A is discharged and forced to ground voltage. This accomplishes the write logic '0' operation. As a result, node A stores the logic '0'.

5. Conclusions

In this paper, we proposed a novel 5T SRAM cell structure. During a write operation, by means of sizing the transistor N11 smaller to avoid the difficulty in writing a logic '1' operation, while without impeding the reading operation. Further, during a read operation, the source voltage of transistor N11 is set to a negative voltage to speed up the reading speed. Moreover, with the standby start-up circuit design, the cell can be switched to the standby mode quickly, thereby improving the standby efficiency and consume lower standby current. Finally, a transistor count comparison is carried between a 1024×1024 SRAM array of an existing six-transistor technology and the proposed technology. It is shown that the total transistor count of the proposed technology can be reduced by 16.6% while maintaining comparable performance.

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