Design of High Performance Single-Port 5T SRAM Cell with Reduced Leakage Current

[1,*] Chien-Cheng Yu and [2]Ming-Chuen Shiau

Abstract

In this paper, a novel single-port five-transistor (5T) Static Random Access Memory (SRAM) cell and associated read/write assist are proposed. Amongst them, a word line suppression circuit is to provide a voltage of the respective connected word line to be lower than or equal to the power supply voltage V_{DD}, so that the read/write-ability of the cell can be improved, and the half-selected cells disturbance can be reduced. Furthermore, a voltage control circuit is coupled to the sources corresponding to the driver transistors of each row memory cells. This configuration is aimed to control the source voltages of driver transistors under different operating modes. In addition, a pre-charging circuit is designed to pull up the bit line BL of a selected column to the voltage V_{DD} before the read operation. Finally, with the standby start-up circuit design, the memory cell can be rapidly switched to the standby mode, thereby reducing leakage current in standby.

Keywords: Read/write assist circuitry, Standby start-up circuit, Static random access memory, Word line suppression circuit.

1. Introduction

In the deep submicron technology, a large number of memory cells are used in products such as microprocessors, communications chips and system on a chip (SOC) applications. Non-volatile memory retains its data even when power is not applied. However, volatile memory requires energy to retain its data. Usually, a volatile memory is classified into a DRAM (dynamic random access memory) and an SRAM (static random access memory) according its respective data storage capability. DRAM is advantageous for its small size, but requires periodic refresh to prevent data loss due to current leakage. However, SRAM requires no refreshing and will maintain its information as long as it has sufficient power supplied. This is due to the fact that the SRAM cell includes flip-flop circuitry internally that does not require refreshing, but occupies a large chip area.

An SRAM cell has three modes of operation, namely read, write and standby [1]. SRAM cells use a write operation to store data in the cell and a read operation to sense the data stored in the cell. Both read and write operations to the selected SRAM cells are performed by decoding the address to result in a word line being activated. The data stored in the cells may be corrupted when the cells are read. This problem arises from the fact that a higher voltage on the bit line is coupled to a lower voltage in the cell, causing the bit line voltage to drop and the cell voltage to rise. Further, a concern associated with the write operation is that it is relatively difficult to write a logical '1' to the cell if the cell currently stores a logical '0'. Accordingly, the SRAM cell should provide less likely to be corrupted when the cell is read and more reliable when the cell is written [2].

As integrated circuits become smaller and denser as power consumption specifications for battery powered integrated circuits decrease, along with power supply voltages, the present SRAM cell designs are increasingly inefficient in both silicon area used and power consumed [3]. Therefore, there is a crucial need for a low leakage and highly robust SRAM design. Leakage current from a memory cell can cause unnecessary power consumption, especially during a standby mode. Recent research has shown that the leakage current will become even more than the dynamic current in the overall power consumption [4]. Typically, there are three major sources of leakage in a MOS transistor, namely subthreshold leakage, gate leakage, and reverse bias junction leakage [5]. Amongst them, the Gate-Induced drain leakage (GIDL) is an unwanted short-channel effect that occurs at higher drain biases in an overdriven off state of a MOS transistor. However, the Drain-induced barrier lowering (DIBL) is a short-channel effect in MOS transistors referring originally to a reduction of threshold voltage of the transistor at higher drain voltages. With the CMOS technology scales down to 90 nm and below, the power consumption caused by leakage currents is becoming a significant part of the global power consumption [6]. Therefore, it would clearly be desirable to provide a design for an SRAM cell that has less leakage current than traditional designs when the cell is in standby.

*Corresponding Author: Chien-Cheng Yu
(E-mail: jenkenyu@gmail.com)
[1] Department of Electronic Engineering, Hsiuping University of Science and Technology, Taichung, Taiwan
[2] Department of Electrical Engineering, Hsiuping University of Science and Technology, Taichung, Taiwan

The remainder of this paper is organized as follows. Section 2 presents a brief description of standard 6T and 5T SRAM cell topologies. The proposed single-port 5T SRAM cell with integrated read/write assist is described in Section 3. The simulation results of the proposed 5T SRAM cell are discussed in Section 4. Last section is a conclusion and summary for the paper.

2. Existing 6T and 5T SRAM Cell Topologies

The standard 6T SRAM is made of two cross-coupled inverters (INV-1 and INV-2) and two access transistors (MA1 and MA2), connecting the cell to the bit lines (BL and BLB), as shown in Fig. 1 [7]. The pair of cross-coupled inverters is formed by load transistors (MP1 and MP2) and driver transistors (MN1 and MN2) that are stronger than the access transistors. More specifically, the cross-coupled inverters of the memory cell have two storage nodes A and B which function to store either logic '1' or logic '0'. The gates of the access transistors are connected to a word line WL, and a rising transition on the word line is to assert the access transistors during a read or a write operation. At the end of the read and write operations, the word line WL is de-asserted to allow the cross-coupled inverters to function normally and hold the logic state of the storage nodes.

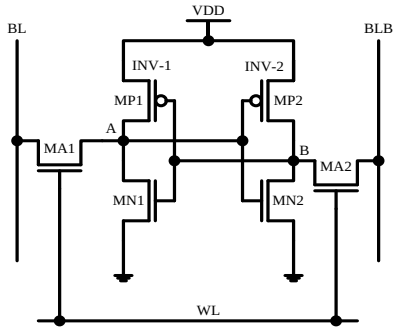

Figure 1: Circuit diagram of the standard 6T SRAM cell.

A concern associated with the read operation is that because of the back-to-back connection of cross-coupled inverters, a regenerative action develops and node A is pulled high, which results in the destruction of contents in the bit cell. Especially, when a logical '0' is stored initially, the voltage rising in the cell may corrupt the data stored. Therefore, it is desirable to keep the voltage at the storage node that has a logical '0' stored from rising above the trip-voltage of the inverter. To provide a non-destructive read operation, the cell ratio (CR) is conventionally varied from 1 to 2.5 [2], where the W/L ratio of the driver transistor to the access transistor is referred as the cell ratio. On the contrary, for a successful write operation, it may be necessary that the access transistors should be very conductive to force the cross-coupled inverters to change its equilibrium condition. However, the access transistor should have a reduced conductivity for good stability in reading and standby operations. These two requirements impose contradicting requirements on cell transistor sizing. To improve the read-ability of an SRAM cell, cell ratio can be increased, while a lower pull-up ratio is desirable to improve the cell write-ability, where the ratio of the load transistor to the access transistor is referred as the pull-up ratio (PR).

Figure 2 is a circuit diagram of a traditional 5T SRAM cell [8]. As shown in Fig. 2, the access transistor MA2 and bit line BLB in Fig. 1 have been removed to provide a five-transistor configuration. The removal of such access transistor allows for an area savings up to 20-30% compared to the standard 6T SRAM cell, while its power consumption is substantially reduced by one half [9]. Although the traditional 5T SRAM cells offer such significant reductions in power consumption, a serious drawback shows that it is difficult to write '1' to the cells. In detail, when the bit line BL is set high and the word line WL is asserted, the transistors MA1 and MN1 fight each other. To guarantee a correct write operation to occur, it is important to note that the storage node A must be pulled up (or down) above (or below) the trip-voltage of INV-2 when the word line WL is logic high, otherwise a write failure will occur. In more detail, writing a logical '1' to a cell when initially a logical '0' is stored, the low storage node A of the cell must be pulled up by the pre-charged bit line BL above the trip-voltage of INV-2.

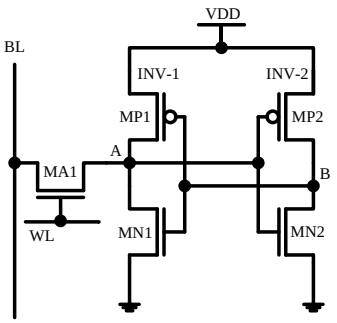

Figure 2: Circuit diagram of the traditional 5T SRAM cell.

In order to resolve the write '1' issue of the traditional 5T SRAM cells, several techniques have been developed. Some of these techniques rely on boosted word line voltage [10-12], reducing the supply voltage V_{DD} [8-9], [13-14], sizing cell transistors [15-17], reduced bit line voltage [18-19], and raising the source voltage V_{SS} [20-22]. However, each of these techniques may cause a reduction in the drive current of the transistors and in the operating speed of the cell, or has increased memory cell area and a degradation in the manufacturing accuracy, or requires generation of a voltage above the operating voltage, or requires a more complicated circuit design and more complicated device process. Hence, there is a need for an effective technique to improve the write-ability of 5T SRAM cells which suffer from inability to write '1'.

3. The Proposed 5T SRAM Cell

3.1 The Proposed 5T SRAM Cell Configuration

The proposed 5T SRAM cell with read/write assist is shown in Fig. 3. The read/write assist includes a word line suppression circuit, a pre-charging circuit, a standby start-up circuit and a voltage control circuit. Amongst them, the word line suppression circuit is to provide a voltage of the selected word line when the respective word lines are in an active state. The proposed 5T SRAM cell is formed using CMOS technology, which is integrated into a memory array that includes m rows and n columns. Each row is identified with a word line WL, and each column is identified with a bit line BL of the memory. One of the memory cells is located at each intersection of a word line WL and a single bit line BL. In this work, each word line is simply connected to the word line suppression circuit, and a voltage level to change circuit for changing the voltage level of the selected word line is not required, suppressing increase in layout area of the word line drivers. Unlike the traditional 5T SRAM cell in Fig. 2, a pull-down word line voltage V_{DD}-V_{TN51} is applied to the word line control signal WLC of the selected row cells to improve the cell read- and write-ability. In detail, the word line suppression circuit weakens the access transistor N13 so that the voltage drops across the transistor N13, the voltage drops between the transistor N13, and the driver transistor N11 reduces, thereby increasing the read-ability. It is worth noting that the word line control signal WLC of the selected cell provides a voltage V_{DD}-V_{TN51} during a read operation, wherein V_{TN51} is the threshold voltage of the transistor N51. However, the power supply voltage V_{DD} is supplied during a write operation. In this suppression circuit, the read signal R and the inverse write signal /W can be achieved from the memory read/write control pin. When the signal R is at logic high, it indicates that the cell is in a read operation; however, the inverse write signal /W is at logic low and indicates a write operation. And the inverse signal of the read/write control pin is same as the inverse read/write control signal /RW. The voltage level of the signal WLCs under different operating modes is shown in Table 1. It is worth noting that by using the word line suppression circuit to pull down the voltage of the signal WLC in a selected row cells to V_{DD}-V_{TN51} during a read operation, it reduces the half-selected cells disturbance.

Table 1: Voltage level of the signal WLC under different operating modes

cells	WL	R	$\overline{W}$	$\overline{RW}$	WLC	mode
selected row cells	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}-V_{TM51}	read
non-selected row cells	0	V_{DD}	V_{DD}	V_{DD}	0	read
selected row cells	V_{DD}	0	0	V_{DD}	V_{DD}	write
non-selected row cells	0	0	0	V_{DD}	0	write
each cell	0	0	V_{DD}	0	0	non-access

In addition, the pre-charging circuit is connected to the bit line BL in each column. The function of the pre-charging circuit is to pull up the bit line BL of a selected column to V_{DD} before the read operation. Furthermore, the standby start-up circuit is to enable the SRAM cell to quickly switch to the standby mode, and thus effectively enhance the standby performance. Refer to Fig. 3, when the write control signal WC is at logic low, the voltage of node C will be equal to that of the inverse standby control signal /S. On the contrary, when the write control signal WC is at logic high, the voltage of node C will be equal to that of the voltage of the control signal S. Thereby, in a standby operation, it effectively avoids the error writing caused by unexpected factors. Wherein, in the non-read mode, the voltage of the read control signal RC is set to the voltage RGND to prevent the leakage current caused by the transistor N24 in the non-read mode. Furthermore, during the initial period in standby, the standby start-up circuit is designed to rapidly charge the parasitic capacitance of the node L1 to the voltage V_{TN23}.

Particularly, during a write operation, the voltage V_{L1} is set to $V_{GS(N23)}$, and that of node L2 (V_{L2}) is set to the ground voltage, where $V_{GS(N23)}$ is the threshold voltage of the transistor N23. Thus, the issue concerning the difficulty of writing '1' can be resolved. In addition, during a standby operation, both V_{L1} and V_{L2} are set to $V_{GS(N23)}$ to reduce the

leakage current in standby. Table 2 summaries the operating conditions under different operating modes. In Table 2, the write control signal WC can be achieved by performing the AND operation on the write signal W and its corresponding word line signal WL. And the read control signal RC can be achieved by performing the AND operation on the read signal R and its corresponding word line signal WL.

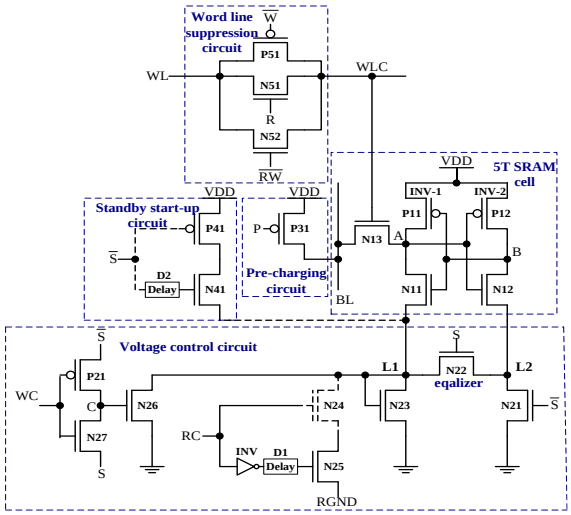

Figure 3: Circuit diagram of the proposed 5T SRAM cell.

Table 2: The operating conditions under different operating modes

RC	WC	S	V_{L1}	V_{L2}	mode
RGND	0	0	$V_{GS(N23)}$	0	write
V_{DD}	0	0	RGND	0	read
RGND	0	V_{DD}	$V_{GS(N23)}$	$V_{GS(N23)}$	standby
RGND	0	0	0	0	hold

An advantage of the proposed design over the traditional 5T SRAM cell is that it is unnecessary to boost the write line signal above V_{DD} to speed up the read operation. Furthermore, this design has the additional advantage to increase current through the driver transistor during a read operation, and consequently lower read delay.

3.2 Write Operation

Refer to Fig. 3, prior to the write operation is performed, the write control signal WC is at logic low, the transistor P21 is turned on, and the transistor N27 is turned off. Thereby, the node C is at logic high and thus to turn on the transistors N26, as the voltage V_{L1} is pulled down to the ground voltage. However, during the write operation, the signal WC is at logic high, the transistors P21 is turned off, and the transistor N27 is turned on. Subsequently, the node C is at logic low and thus to turn off the transistors N26, as the voltage V_{L1} is set to $V_{GS(N23)}$. Thus, the issue concerning the difficulty of writing '1' can be resolved. Figure 4 shows the simplified circuit diagram during the write operation.

The transients associated with a writing operation are in detail described below. Firstly, let us consider the write '0' operation. Prior to the write '0' operation, the voltage V_{BL} and signal WLC are at logic low. During the write '0' operation, if a '0' is stored previously, the signal WLC transitions from a logic low to a logic high. As the signal WLC exceeds the threshold voltage of transistor N13 (V_{TN13}), transistor N13 is turned on. Subsequently, due to the fact voltage V_{BL} is at logic low, the voltage V_A remains at the ground voltage. On the other hand, if a logical '1' is stored previously, the signal WLC transitions from a logic low to a logic high. As the signal WLC exceeds the threshold voltage V_{TN13}, transistor N13 is turned on. Subsequently, due to the fact voltage V_{BL} is at logic low, the node A and node L1 will be discharged to ground until the end of the write '0' operation.

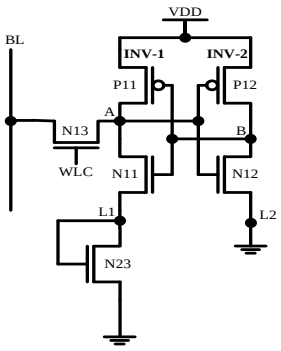

Figure 4: Simplified circuit diagram during the write operation.

Secondly, consider the write '1' operation. Prior to the write '1' operation, the signal WLC is at logic low, and the voltage V_{BL} is at logic high. During the write '1' operation, if a '1' is stored previously, the signal WLC transitions from a logic low to a logic high. As the signal WLC exceeds the threshold voltage V_{TN13}, transistor N13 is turned on. Subsequently, due to the fact voltage V_{BL} is at logic high, and transistor P11 remains on, the voltage V_A will remain at the power supply voltage V_{DD} until the end of the write operation. On the other hand, if a '0' is stored previously, the signal WLC transitions from a logic low to a logic high. Subsequently, with the increase of the signal WLC, the voltage V_A will rise. As the signal WLC exceeds the threshold voltage V_{TN13}, transistor N13 is turned on. Subsequently, due to the fact voltage V_{BL} is at logic high and transistor N11 remains on, and the voltage V_B remains at a voltage close to the power supply voltage V_{DD}, the transistor P11 remains off. For a successful write operation, it is desirable to pull down the voltage V_A (or V_B) which has a stored value '1' below the

trip-voltage of the inverter. Meanwhile, the write initial transient voltage V_{AW} of node A must satisfy the following equation:

$$V_{AW} = V_{DD} \times \frac{R_{N11} + R_{N23}}{R_{N11} + R_{N13} + R_{N23}} > V_{TN12} \quad (1)$$

where V_{TN12} is the threshold voltage of the transistor N12, R_{N11}, R_{N13} and R_{N23} are the on-resistance of transistors N11, N13 and N23, respectively. Consequently, the write '1' problem associated with the traditional 5T SRAM cell can be avoided.

Now, the transistor N13 is still in the saturation region and the transistor N11 in the triode region. Although R_{N13} may be greater than R_{N11}, the NMOS diode N23 can provide a voltage $V_{GS\,(N23)}$ at node L1. As a result, the voltage V_A will rise up due to the voltage division along the driver and access transistors. When the voltage exceeds a threshold, it causes the bit to flip due to regenerative feedback. Hence, the write '1' operation is completed. Consequently, the write '1' problem associated with the traditional 5T SRAM cell can be resolved. It is worth noting that the voltage V_{L1} is $V_{GS\,(N23)}$ when writing a logical '1' to a logical '0' is stored. After completing the write '1' operation, the voltage V_{L1} will be discharged to ground via transistor N26.

3.3 Read Operation

Figure 5 shows the simplified circuit diagram during the read operation. Prior to initiating a read operation, the bit line BL is pre-charged to V_{DD}, and the standby start-up control signal S, the write control signal WC and the read control signal RC are at logic low; thereby, the transistors P21 and N25 are turned on, and the transistors N24 and N27 are turned off, as the voltage of node C is at logic high and subsequently turn on the transistor N26. This leads to the voltage V_{L1} pulled down to ground.

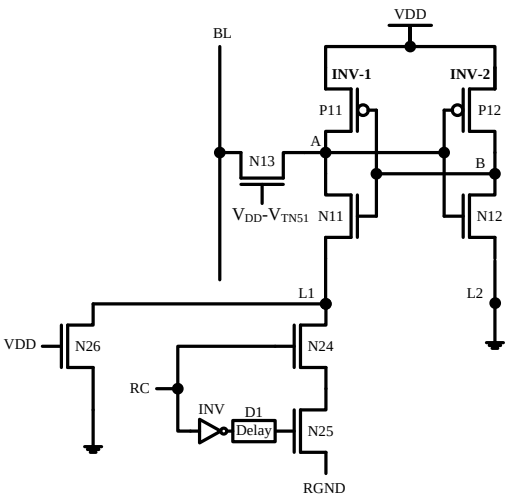

Figure 5: Simplified circuit diagram during the read operation.

During the read operation, the read control signal RC is at logic high, and transistor N24 is turned on. At this time, since transistor N25 would continue to conduct, the voltage V_{L1} will be pulled down to a negative voltage RGND as shown in Fig. 6. Under this circumstance, the negative voltage RGND can effectively improve the reading speed. It is noted that the time interval is measured as the time taken from a high on the read control signal RC to the state of the transistor N25 turned off. This time interval can be adjusted by the falling time of the inverter INV and the delay time of the delay circuit D1. Furthermore, the transistor N26 is always on during the read operation.

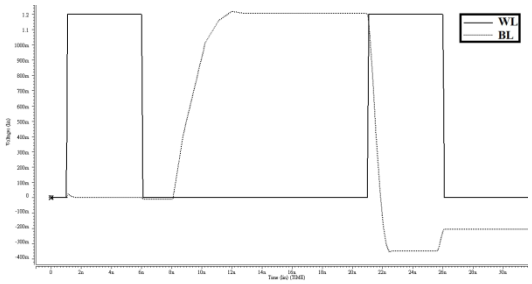

Figure 6: Voltage level waveforms during a read operation.

The transients associated with a reading operation are in detail described below. Firstly, let us consider the read '1' operation. Before the read '1' operation occurs, the transistor N11 is off and the transistor N12 is on; and the voltage V_A and the voltage V_B are V_{DD} and ground, respectively. And the voltage V_{BL} is equal to V_{DD} due to the pre-charging circuit. During the read operation, since the voltage V_{WLC} is V_{DD}-V_{TN51}, the transistor N13 is turned on. Thereby, the voltage V_{BL} can be effectively kept at V_{DD} until the end of the read '1' operation. It is worth noting that due to the voltage RGND equaling to V_{L1}, in order to effectively reduce the half-selected cell disturbance and effectively reduce the leakage current during the read '1' operation, the absolute value of the voltage RGND may be set to be smaller than the voltage V_{TN11} in reading '1', i.e.,

$$|RGND| < V_{TN11} \quad (2)$$

where |RGND| denotes the absolute value of the voltage RGND, and V_{TN11} is the threshold voltage of transistor N11.

Secondly, consider the read '0' operation. Before the read '0' operation is performed, the transistor N11 is on and the transistor N12 is off; and the voltage V_A and the voltage V_B are grounded, respectively. And the voltage V_{BL} is equal to V_{DD} due to the pre-charging circuit. During the read '0' operation, since the voltage V_{WLC} is V_{DD}-V_{TN51}, the

transistor N13 is turned on. Meanwhile, the initial transient voltage V_{AR} of the node A must satisfy the following equation:

$$V_{AR} = V_{DD} \times \frac{R_{N11} + (R_{N24} + R_{N25}) \| R_{N26}}{R_{N13} + R_{N11} + (R_{N24} + R_{N25}) \| R_{N26}} + RGND \times \frac{(R_{N11} + R_{N13}) \| R_{N26}}{R_{N24} + R_{N25} + (R_{N11} + R_{N13}) \| R_{N26}} \times \frac{R_{N13}}{R_{N11} + R_{N13}} < V_{TN12} \quad (3)$$

where V_{AR} is the initial transient voltage of node A, V_{TN12} is the threshold voltage of transistor N12, R_{N11}, R_{N13}, R_{N24}, R_{N25} and R_{N26} are the on-resistance of transistors N11, N13, N24, N25 and N26, respectively.

It is worth noting that the voltage RGND is designed to be lower than the ground voltage, and its absolute value is designed to be smaller than the voltage V_{TN11}. Furthermore, during the read '0' operation, the voltage V_{WLC} is set to V_{DD}-V_{TN51} in the paper. This design can increase R_{N13} to satisfy the Equation (3) and can reduce the half-selected cell disturbance in read '0' operation.

3.4 Standby Operation

Refer to Fig. 3, prior to the standby operation is performed, the inverse standby control signal /S is at logic high, thus the transistor P41 is turned off, and the transistor N41 is turned on. And, during the standby operation, the signal /S is at logic low to turn on the transistor P41 and to turn off the transistor N21. In addition, the high standby control signal S is to turn on the transistor N22 which acts as an equalizer. Consequently, with the conduction of the transistor N22, both the V_{L1} and V_{L2} are equal to the voltage V_{TN23}. It is worth mentioning that node L1 can be rapidly charged to V_{TN23} at the initial period of the standby mode since transistor N41 remains on, and thereby improving the standby efficiency. Note that the initial period is determined as the time taken from a low on the signal /S to the off state of transistor N41. This time interval can be adjusted by the delay time of the delay circuit D2. It is worth noting that after the initial period of the standby mode, transistor N41 is turned off, and no current flows. Figure 7 shows the simplified schematic of the proposed design during the standby mode.

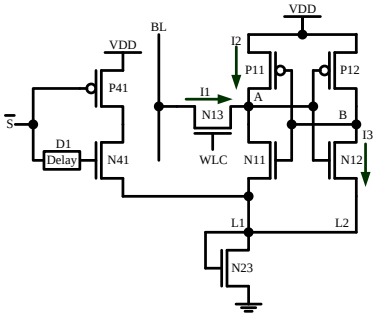

Figure 7: Simplified circuit diagram during the standby operation.

4. Simulation Results

In this paper, the read operation is initiated by enabling the word line control signal WLC and connecting the pre-charged bit line BL to the storage node A. If the word line control signal WLC is reduced, the voltage V_A is also reduced during the read operation. In more detail, during the read operation, the word line control signal WLC in a selected row cell is set to a voltage V_{DD}-V_{TN51}. Thereby, the gate voltage of the access transistor N13 of the selected cell is reduced to decrease its current driving power, and thus leads to prevent data corruption in the read operation. On the contrary, during the write operation, the word line control signal WLC in a selected row cell is set to a power supply voltage V_{DD}, and the word line control signal WLCs for the non-selected row cells are set to a ground voltage similar to that in a read operation, resulting that a static noise margin in the read operation is improved, and a write margin is ensured. Apart from these modes, the word line control signal WLCs for the non-access cells are set to a ground voltage.

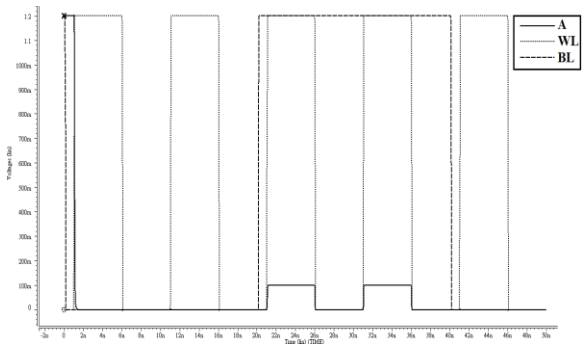

Figure 8: Transient waveforms of a write failure in the traditional 5T SRAM cell.

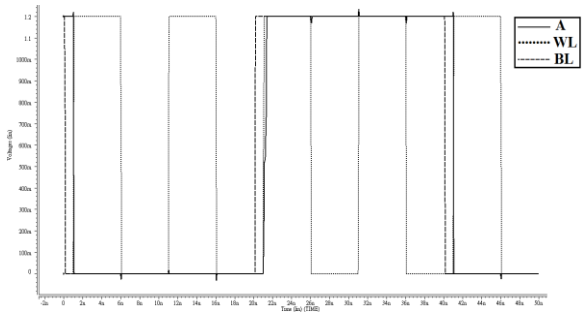

Figure 9: Transient waveforms of a successful writing in the proposed 5T SRAM cell.

In the traditional 5T SRAM cell, the access transistor MA1 is less conductive than the driver transistor MN1, thereby making it more difficult to write a logical '1' to cell over a logical '0' is stored. Figure 8 shows the simulated waveform of a write '1' failure. To evaluate performance, different SRAM cell structures discussed in this paper are simulated using a 90nm CMOS technology. All simulations are carried out at nominal conditions: V_{DD}=1.2V and at room temperature. The simulated waveform of a successful writing in the proposed 5T SRAM cell is shown in Fig. 9. It is evident that the proposed 5T SRAM cell provides an efficient solution to the write '1' issue, that is, the proposed 5T SRAM cell enables a logical '1' to be easily written to the SRAM cell, as compared with the traditional 5T SRAM cells.

Upon standby mode shown in Fig. 7, the voltage V_A remains at V_{TN23}, the voltage V_{WL} is set to the ground voltage and V_{BL} is set to V_{DD}, respectively. Therefore, the gate-source voltage V_{GS} of transistor N13 is negative. In contrast, the V_{GS} of transistor MA1 in Fig. 1 is equal to zero. For NMOS transistors, according to the GIDL effect, the sub-threshold current at V_{GS}= -0.1 is approximately 1% of that at V_{GS}=0. Accordingly, the leakage current I1 flows through transistor N13 caused by the GIDL effect is much smaller than that of flowing through transistor MA1 in Fig. 1. Furthermore, the drain-source voltage V_{DS} of transistor N13 is V_{DD}-V_{TN23}, whereas the voltage V_{DS} of transistor MA1 in Fig. 1 is V_{DD}. According to the DIBL effect, the leakage current I1 flowing through transistor N13 is also less than that of flowing through transistor MA1 in Fig. 1. As a result, the leakage current flows through transistor N13 is much smaller than that of flowing through transistor MA1 in Fig. 1. Next, the source-drain voltage V_{SD} of transistor P11 is V_{DD}-V_{TN23} in contrast to the V_{SD} = V_{DD} of transistor MP1 in Fig. 1. According to the DIBL effect, the leakage current I2 flowing through transistor P11 will be less than that of flowing through transistor MP1 in Fig 1. Thus, the base-source voltage V_{BS} of transistor N12 is negative, and the drain-source voltage VDS of transistor N12 is V_{DD}-V_{TN23}. On the contrary, the V_{BS} of transistor MN2 in Fig. 1 is zero, and the V_{DS} of transistor MN2 is V_{DD}. According to the body effect and DIBL effect, the leakage current I3 flowing through transistor N12 is much smaller than that of flowing through transistor MN2. From the above analysis, it can be seen that the proposed 5T single-port SRAM has a lower leakage current compared with the standard 6T SRAM. Table 3 shows a comparison between the simulated standby leakages of the traditional 6T SRAM cell and the proposed 5T SRAM cell using 90 nm CMOS technology. For each cell, the total leakage current flow, which is the sum of I1, I2 and I3 of all transistors is estimated.

Table 3: Leakage current comparison

Corner model	Proposed 5T SRAM (pA)	Standard 6T SRAM (pA)	Improvement (%)
TT	3.1655	22.2203	85.7
SS	1.2369	1.6191	23.6
FF	61.5317	309.2402	80.1

As it can be seen from Table 3, compared with the standard 6T SRAM cell in different corner models, the standby leakage current of the proposed design is significantly reduced 85.7%, 23.6% and 80.1%, respectively.

5. Conclusions

In this paper, the word line suppression circuit is used to limit the selected word line voltage to a value lower than the power supply voltage. Therefore, the voltage level of the selected word line can be low in the read operation, and the conductance of the access transistor of the memory cell is so small that the read-ability is improved, and the memory cell can stably read data. An advantage of this circuit design over the traditional 5T SRAM cell is that it is not necessary to boost the write line signal above V_{DD} to speed up the read operation. Furthermore, this design has the additional advantage of increasing current through the driver transistor during a read operation, and consequently lowers read delay. Besides, this paper facilitates efficient data writing to an SRAM cell, particularly if a logical '0' stored in the cell is to be overwritten by a logical '1'. Additionally, with the design of standby start-up circuit, the memory cell can be rapidly switched to the standby mode, thereby reducing leakage current and maintaining high performance.

Simulation results for the proposed 5T cell design confirm that there is conspicuous improvement over the standard 6T SRAM cell while it allows writing '1' on the cell with read/write assist. In addition, with the proposed read/write assist it leads to less standby leakage in different corners compared with the standard 6T SRAM cell. It demonstrates that the proposed 5T SRAM cell is capable of delivering high performance with reduced leakage current, and it can be utilized in many applications that are desirable to maintain high-speed and reduce power consumption.

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Chien-Cheng Yu received the B.S. and M.S. degrees from Feng Chia University and National Taiwan Normal University, respectively. He is currently an Assistant Professor with the department of Electronic Engineering at Hsiuping University of Science and Technology, Taichung, Taiwan. His current research interests include design and analysis of high speed, low power integrated circuits and low-voltage low-power embedded SRAM circuit design.

Ming-Chuen Shiau received the B.S., M.S. and Ph.D. degrees in Electronic Engineering from National Chiao Tung University, Hsinchu, Taiwan. He is currently a Professor with the department of Electrical Engineering at Hsiuping University of Science and Technology, Taichung, Taiwan. His current research interests include low-power digital circuit design, SRAM design and low-voltage embedded memory circuit design.